A Two-Stage Differential Input Single-Ended Output OpAmp Design

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***Abstract*—A two-stage differential input single ended output OpAmp design with 180 nm technology is presented in this paper. An OTA topology is implemented in the first stage of the circuit, and an CMOS push-and-pull inverter functions as the second stage. This design achieved phase margin of over 90°, ADM0 of 2470 V/V, ACM0 of 0.094 V/V, slew rate of 15.56 V/us, voltage swing of 800.30 mVpp, and a low power consumption of 464.4 uW.**

***Index Terms*—operational amplifier, OTA, differential pair, analog CMOS design, frequency compensation**

I. Introduction

This project is meant to design a differential input single-ended output CMOS OpAmp for a specific application where the OpAmp will be used as a buffer.

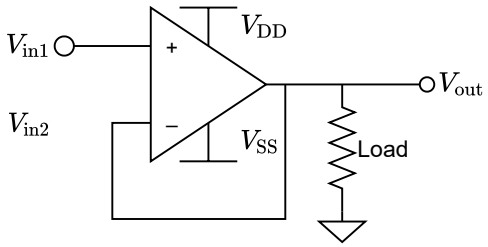

Fig. 1. OpAmp in unity-gain feedback (i.e., unity buffer)

II. Spec Analysis and OpAmp Design Consideration

The OpAmp design is constrained by the following design specs.

In this design with $0.18\,\mu\mathrm{m}$ CMOS technology, only NMOS, PMOS transistors, capacitors, and resistors can be used.

III. OpAmp Design and Optimizations

A two stage amplifier topology is used for this design, as is shown in Figure 2. The first stage is an OTA differential pair, and the second stage is an inverter.

According to [4], for N-type MOSFET, we have

$$I_{\mathrm{D}} = \mu_n C_{\mathrm{ox}} \frac{W}{L}\left[(V_{\mathrm{GS}} - V_{\mathrm{TH}})V_{\mathrm{DS}} - \frac{1}{2}V_{\mathrm{DS}}^2\right] \tag{1}$$

When the transistor enters saturation region, we have

Specification Name	Requirement
Process	$0.18\,\mu\mathrm{m}$
V_{DD}	$1.8\,\mathrm{V}$
V_{SS}	$0\,\mathrm{V}$
Load	$1\,\mathrm{pF}$
ADM0*	$\geq 1\,000\,\mathrm{V\,V^{-1}}$
ACM0**	$\leq 0.1\,\mathrm{V\,V^{-1}}$
Phase margin	$\geq 60°$
Unity gain frequency	$\geq 100\,\mathrm{MHz}$
Slew rate	$\geq 10\,\mathrm{V}/\mu\mathrm{sec}$
Nominal input and output common-mode voltage	$0\,\mathrm{V}$
Output voltage swing (differential peak to peak)	$\geq 800\,\mathrm{mVpp}$
Power	Minimum ($\leq 1\,\mathrm{mW}$)

* low-frequency open-loop small-signal gain
** low-frequency open-loop small-signal common-mode gain

TABLE I
The design specifications

$$I_{\mathrm{D,max}} = \frac{1}{2}\mu_n C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 \tag{2}$$

Equation (2) forms the basis of our analysis. Consequently, we may derive the three expressions of the transconductance of the transistors.

$$g_{\mathrm{m}} = \begin{cases} \mu_n C_{\mathrm{ox}} \dfrac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}}) \\ \sqrt{2\mu_n C_{\mathrm{ox}} \dfrac{W}{L} I_{\mathrm{D}}} \\ \dfrac{2I_{\mathrm{D}}}{V_{\mathrm{GS}} - V_{\mathrm{TH}}} \end{cases} \tag{3}$$

For more precise analysis, channel length modulation must be included, and we have

$$r_o \approx \frac{1}{\lambda I_{\mathrm{D}}} \tag{4}$$

A. Deciding biasing current

The power consumption is $\leq 1\,\mathrm{mW}$, and the total voltage is $V_{\mathrm{DD}} = 1.8\,\mathrm{V}$, hence the total current should be

$$I_5 \leq \frac{P_{\mathrm{total}}}{V_{\mathrm{DD}}} = \frac{1\,\mathrm{mW}}{1.8\,\mathrm{V}} = 555.56 \tag{5}$$

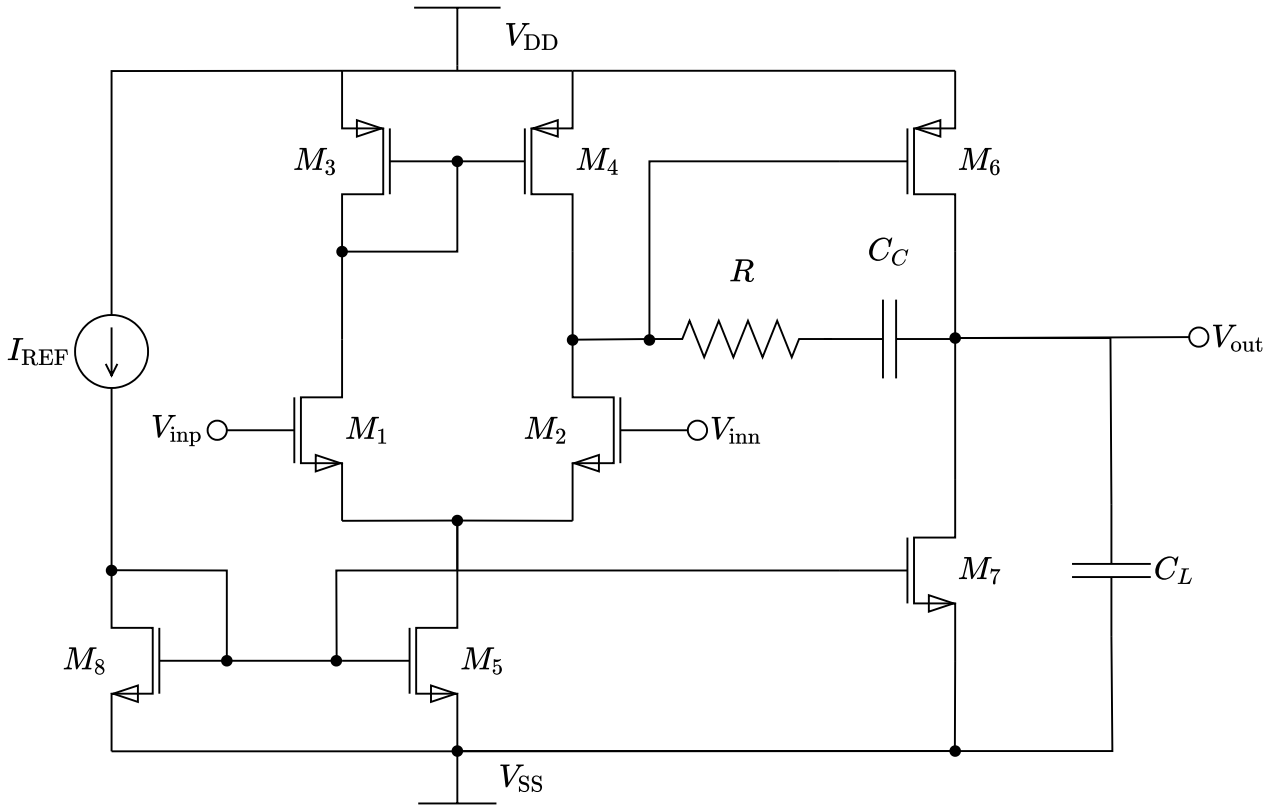

Fig. 2. The schematic of the circuit design

The total current is the sum of the current through M_8, $M5$, and M_7, while M_5 and M_8 together form current mirror, and hence the current through M_5 should be multiples of M_8, and is further determined by the length width ratio of the two transistors. Therefore, we may ignore the current through M_8 for temporary, and consider only that of M_5 and M_7.

By experiment, the current flowing through M_7 is approximately two to three times of M_5, we may first set an intermediate value of biasing current for M_5, that is, the total current of the OTA topology, to approximately $80\,\mu\mathrm{A}$.

B. Adjusting DC operating point

The reference current is fixed at $10\,\mu\mathrm{A}$, hence the current mirror has a current gain of 8, and we have

$$I_{\mathrm{out}} = \frac{(W/L)_5}{(W/L)_8} I_{\mathrm{REF}} \implies \frac{(W/L)_5}{(W/L)_8} = \frac{I_{\mathrm{out}}}{I_{\mathrm{REF}}} = 8 \qquad (6)$$

We may then proceed to adjust the width to length ratio, for the transistors to be in saturation. Due to the requirement of our design on voltage swing, and the feedback is directed coupled from the ouput point to the input point, there should be headroom for the overdrive voltage $V_{\mathrm{GS}} - V_{\mathrm{TH}}$, in order to ensure M_1 and M_2 would not enter linear region in the voltage swing.

C. Adjusting output voltage

According to [4], we may increase the voltage at the base to increase the value of V_{TH} to increase the headroom, however, base and source are connected in the common practice of for the purpose of fabrication. Our design is constrained by an input and output common-mode voltage of $0\,\mathrm{V}$ and a V_{DD} of $1.8\,\mathrm{V}$, hence, to reach the maximum voltage swing, we set the DC voltage bias at the output point as $900\,\mathrm{mV}$. Therefore, while maintaining M_6 and M_7 in the saturation region, we need to set the V_{DS} of M_7 to be $0.9\,\mathrm{V}$, that is, set the V_{DS} of M_6 to be $-0.9\,\mathrm{V}$.

D. Fine tuning the gain

After the forementioned optimizations are done, the small signal open loop gain at differential output and low frequency is still under $60\,\mathrm{dB}$, and the common mode gain is $0\,\mathrm{dB}$, for larger the the reuirement of $-20\,\mathrm{dB}$. By our analysis, such phenomena is caused by the gain of the first stage being too small and that in the second stage being too large.

According to the expression of voltage gain for OTA topology, we may increase the transconductance of transistors at the input point to increase differential mode gain. Therefore, we increased the length of M_1 and M_2 to increase the transconductance, and decreased the length of M_6 in the second stage to decrease the gain of the second stage.

After the adjustment, the requirement on open loop gain is satisfied. Since the headroom at the input point is reserved and

Dimension	Transistor							
	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8
W L	14.4 µm 720 nm	14.4 µm 720 nm	$4 \times 3 = 12$ µm 190 nm	$4 \times 3 = 12$ µm 190 nm	$4 \times 25 = 100$ µm 4 µm	$8 \times 12.8 = 102.4$ µm 500 nm	$5 \times 7.6 = 38$ µm 250 nm	4 µm 960 nm
$\frac{W}{L}$	20	20	63.16	63.16	25	204.8	152	4.17

TABLE II
THE DIMENSION OF THE TRANSISTORS

the biasing current is sufficiently large, output voltage swing and the slew rate also reaches the requirement. Then, R_1 and C_1 are tuned to increase RC and hence push the pole to the left to meet the requirement on phase margin. So far, gain-bandwidth gain is also satisfied.

E. Devices parameters

The final design is specified by the parameters of the devices. The dimensions of transistors is presented in Table II. For other devices, we have $R = 3\,\text{k}\Omega$, $C_C = 1.5\,\text{pF}$, and $I_{\text{REF}} = 10\,\mu\text{A}$.

IV. Simulation Result and Analysis

A. Stability and phase margin

According to Fig. 3, the phase crossover point PX at which the phase decrease $180\,\text{deg}$ is higher than the gain crossover point GX at which the gain is $0\,\text{dB}$. By the Buckhausen Stability Criterion ([4]), our circuit design functions stably.

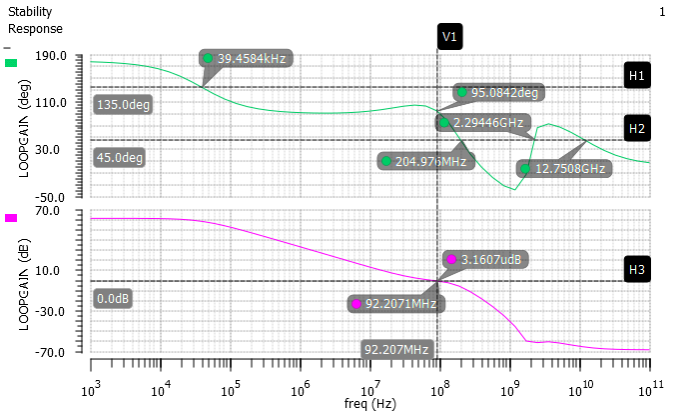

Fig. 3. Frequency response of the closed-loop system

The phase margin of the circuit is $95.084\,2°$, which is greater than $60°$.

B. Poles and zeros

The circuit topology of our design has two stages, and the frequency response of which is determined by two poles and zeros together.

To achieve a phase margin of $60\,\text{deg}$, a loading pole p_2 higher than 2.2 times the GB is required. In which, according to [2], the gain bandwidth product is given by

$$\text{GBW} = \frac{g_{\text{m}2}}{2\pi C_c} \tag{7}$$

Therefore, the positions of the poles and zeros demands that C_c should be larger than $0.22C_L$.

Now consider the positions of the two poles, according to [4], the capacitance in the CMOS is shown in Table IV. Furthermore, with DC simulation, we may find the small signal resistance and the transconductance of each transistors, as shown in Tabel III.

Transistor	M_2	M_4	M_6	M_7
$r_{o\text{N}}$ / kΩ	21.4241	15.4178	5.2945	5.3083
g_{m} / S	552.666 µ	518.615 µ	1.793 2 m	2.854 7 m

TABLE III
THE SMALL SIGNAL RESISTANCE AND TRANSCONDUCTANCE OF THE TRANSISTORS

For the parasitic capacitance inside the MOSFETs, we only consider the prominent ones that can be obtained through DC simulation, i.e. C_{GS} and C_{GD}.

The first pole is at

$$\begin{aligned}\omega_{p1} &= \frac{1}{C_c(r_{o2} \parallel r_{o4})} \\ &= \frac{1}{1.5\,\text{pF} \times (21.424\,1\,\text{k}\Omega \parallel 15.417\,8\,\text{k}\Omega)} \\ &= 74.358\,\text{MHz}\end{aligned} \tag{8}$$

The second pole is at

$$\begin{aligned}\omega_{p1} &= \frac{1}{C_L\left(r_{o6} \parallel \dfrac{1}{g_{\text{m}7}}\right)} \\ &= \frac{1}{1\,\text{pF} \times \left(5.294\,5\,\text{k}\Omega \parallel \dfrac{1}{2.854\,7\,\text{mS}}\right)} \\ &= 3.043\,6\,\text{GHz}\end{aligned} \tag{9}$$

The zero is at

$$\omega_z = \frac{1}{RC_c} = \frac{1}{3\,\text{k}\Omega \times 1.5\,\text{pF}} = 222.22\,\text{MHz} \tag{10}$$

The first and second poles are located at the point where the phase decreased by $45\,\text{deg}$ and $135\,\text{deg}$, respectively. The measured first pole varies largely from the theoretical calculation, while the second pole fits the calculation accurately. The reason could be the parasitic capacitance of the CMOS device itself and the effect of the zero.

Capacitance	Cut-off	Operating region Linear	Saturation
C_{GB}	$C_{\mathrm{ox}}WL$	0	0
C_{GD}	$C_{\mathrm{ox}}WL_{\mathrm{D}}$	$\frac{1}{2}C_{\mathrm{ox}}WL + C_{\mathrm{ox}}WL_{\mathrm{D}}$	$C_{\mathrm{ox}}WL_{\mathrm{D}}$
C_{GD}	$C_{\mathrm{ox}}WL_{\mathrm{D}}$	$\frac{1}{2}C_{\mathrm{ox}}WL + C_{\mathrm{ox}}WL_{\mathrm{D}}$	$\frac{2}{3}C_{\mathrm{ox}}WL + C_{\mathrm{ox}}WL_{\mathrm{D}}$

TABLE IV
THE CAPACITANCE IN THE MOSFET

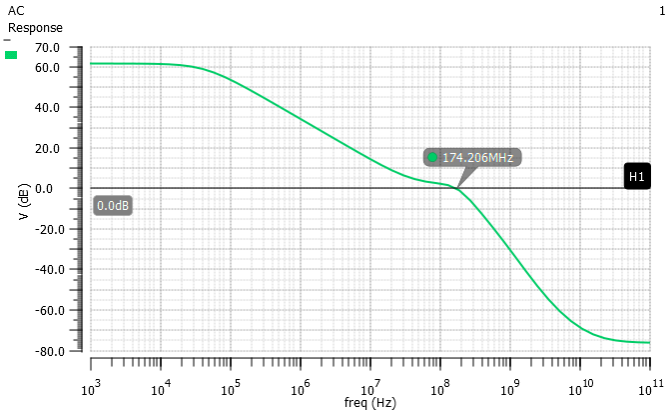

Fig. 4. Open loop gain-bandwidth product

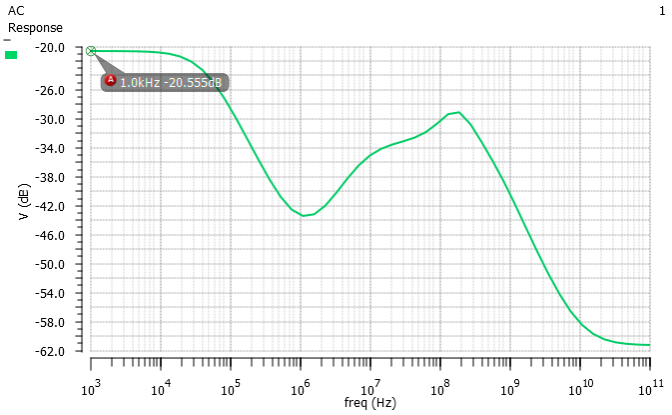

Fig. 5. Common-mode gain

C. Circuit gain

According to Figure 4, the differential mode gain of the circuit is $67.857\,1\,\mathrm{dB}$, and the gain bandwidth product is $174.206\,\mathrm{MHz}$, which is greater than $100\,\mathrm{MHz}$.

Taking the secondary effects into consideration, the two stages gain will be affected by the output impedance of MOSFETs. In the following analysis, we mainly consider the nonidealities introduced by channel length modulation.

The gain at the first stage is given by

$$A_{v1} = -g_{\mathrm{m2}}(r_{o2} \parallel r_{o4}) = -\frac{2g_{\mathrm{m2}}}{I_5(\lambda_2 + \lambda_4)} \tag{11}$$

The gain at the first stage is given by

$$A_{v2} = -g_{\mathrm{m6}}(r_{o6} \parallel r_{o7}) = -\frac{2g_{\mathrm{m6}}}{I_6(\lambda_6 + \lambda_7)} \tag{12}$$

Therefore, according to [3], the theoretical overall gain of our circuit design is

$$A_v = g_{\mathrm{m2}}g_{\mathrm{m6}}(r_{o2} \parallel r_{o4})(r_{o6} \parallel r_{o7}) = 70.656 \tag{13}$$

Which is lower than the gain given by the simulation result, we consider this to be an impact of channel length modulation and bulk effect.

D. Common mode rejection ratio

According to [2], The common mode rejection ratio is given by

$$\mathrm{CMRR} = \frac{A_{v\text{-DM}}}{A_{v\text{-CM}}} = g_{\mathrm{m1,2}}g_{\mathrm{m3,4}}(r_{o1,2} \parallel r_{r3,4})R_{\mathrm{SS}} \tag{14}$$

The common mode gain of our design is presented in Figure 5, which is $-20.555\,\mathrm{dB}$, that is, $0.094\,\mathrm{V/V}$, and is less than $0.1\,\mathrm{V/V}$.

E. Slew rate, voltage swing, and power consumption

The slew rate is presented in Figure 6, which is $15.56\,\mathrm{V\,\mu s^{-1}}$

The voltage swing is presented in Figure 7, which is $800.297\,6\,\mathrm{mV}$.

By DC simulation, the static current of our design is $258\,\mu\mathrm{A}$, hence the power consumption of the amplifier is $464.4\,\mu\mathrm{W}$.

V. CONCLUSION

The circuit functions as expected by our calculation, and satisfies the design requirements properly.

The specifications of our design is presented in Table V, all has reached the desired value.

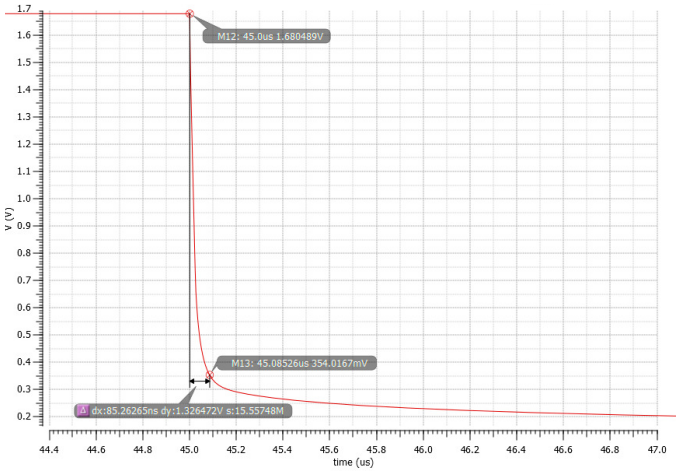

Fig. 6. Slew rate

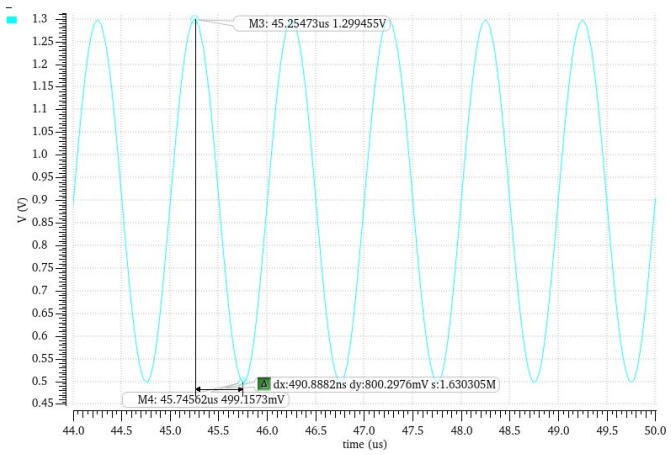

Fig. 7. Voltage swing

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Specification Name	Result Value
V_{DD}	1.8 V
V_{SS}	0 V
Load	1 pF
ADM0*	2 470.899 V V^{-1}
ACM0**	0.094 V V^{-1}
Phase margin	94.465°
Unity gain frequency	204.871 MHz
Slew rate	15.56 V/µsec
Nominal input and output common-mode voltage	0 V
Output voltage swing (differential peak to peak)	800.30 mVpp
Power	464.4 µW

* low-frequency open-loop small-signal gain
** low-frequency open-loop small-signal common-mode gain

TABLE V
THE RESULT SPECIFICATIONS OF OUR DESIGN

Dongshen Zhan (S'22) was born in Hunan Province, China, in 2000. He was preparing to receive the Bachelor degree in microelectronics science and technology from Southern University of Science and Technology (SUSTech), in 2023.

He joined Prof. Pan's group in 2019, where he study in transimpedance amplifier design. In 2021, he started the study CMOS Analog Integrated Circuit Design course at SUSTech. His reserch interests are optical communications integrated circuit and Serdes/TIA circuit.

Guanchao Huang (S'22) was born in Linwu County, Chenzhou City, Hunan Province, China, in 2002. He is an undergradute student in the School of Microelectronics, Southern University of Science and Technology, in Shenzhen, China. He is focused on digital circuit design, and is also interested in other fields in computer science, such as discrete mathematics, embedded systems, machine learning, and software design. He joined Prof. Kai Chen's research group on cryogenic CMOS circuit to learn elements of scientific research.

He is also an exchange student in the University of Notre Dame du Lac, Indiana, United States, mainly study cumputer science.